CLAIMS

We claim:

1. A semiconductor die, comprising:

(a) a semiconductor substrate diffused with a first material to give the substrate a first conductivity type, the substrate having a substrate surface;

(b) a buried layer selectively formed in the substrate surface and diffused with a second material to give the buried layer the opposite conductivity type as the substrate;

(c) an epitaxial layer formed on the substrate surface and on the buried layer, the epitaxial layer having the opposite conductivity type as the substrate, the epitaxial layer having an epitaxial surface distal from the substrate surface;

(d) a first diffused region selectively formed on the epitaxial surface, the first diffused region having the same conductivity type as the epitaxial layer, the first diffused region having a first surface distal from the substrate surface;

(e) a second diffused region selectively formed on the first surface, the second diffused region having the opposite conductivity type as the first diffused region, the first diffused region and the second diffused region combine to form a first semiconductor junction; and

(f) a third diffused region selectively formed on the epitaxial surface remote from the first diffused region, the third diffused region having the opposite conductivity type as the epitaxial layer, the epitaxial layer and the third diffused region combine to form a second semiconductor junction.

2. The semiconductor die of claim 1, in which the first semiconductor junction operates in a reverse avalanche mode while the second semiconductor junction operates in a forward conducting mode during a transient over-voltage event.

3. The semiconductor die of claim 2, in which the epitaxial layer has a higher resistivity than the resistivity of the buried layer and in which a transient current is shunted through the buried layer during the transient over-voltage event.

4. The semiconductor die of claim 1, in which the first diffused region extends from the first surface to the substrate surface.

5. The semiconductor die of claim 4, in which the first semiconductor junction operates in a reverse avalanche mode while the second semiconductor junction operates in a forward conducting mode during a transient over-voltage event.

6. The semiconductor die of claim 5, in which the epitaxial layer has a higher resistivity than the resistivity of the buried layer and in which a transient current is shunted through the buried layer during the transient over-voltage event.

7. A transient voltage suppression device, comprising:

a semiconductor die, the semiconductor die including

(a) a semiconductor substrate diffused with a first material to give the substrate a first conductivity type, the substrate having a substrate surface;

(b) a buried layer selectively formed in the substrate surface and diffused with a second material to give the buried layer the opposite conductivity type as the substrate;

(c) an epitaxial layer formed on the substrate surface and on the buried layer, the epitaxial layer having the opposite conductivity type as the substrate, the epitaxial layer having an epitaxial surface distal from the substrate surface;

(d) a first diffused region selectively formed on the epitaxial surface, the first diffused region having the same conductivity type as the epitaxial layer, the first diffused region having a first surface distal from the substrate surface;

(e) a second diffused region selectively formed on the first surface, the second diffused region having the opposite conductivity type as the first diffused region, the first diffused region and the second diffused region combine to form a first semiconductor junction; and

(f) a third diffused region selectively formed on the epitaxial surface remote from the first diffused region, the third diffused region having the opposite conductivity type as the epitaxial layer, the epitaxial layer and the third diffused region combine to form a second semiconductor junction.

8. The transient voltage suppression device of claim 7, in which the first semiconductor junction operates in a reverse avalanche mode while the second semiconductor junction operates in a forward conducting mode during a transient over-voltage event.

9. The transient voltage suppression device of claim 8, in which the epitaxial layer has a higher resistivity than the resistivity of the buried layer and in which a transient current is shunted through the buried layer during the transient over-voltage event.

10. The transient voltage suppression device of claim 9, in which the second diffused region has a second surface distal from the substrate surface and in which the third diffused region has a third surface distal from the substrate surface, and in which the second surface and the third surface provide first and second external electrical contacts for the transient voltage suppression device.

11. A flip chip, comprising:

a transient voltage suppression device including a semiconductor die, the semiconductor die including

(a) a semiconductor substrate diffused with a first material to give the substrate a first conductivity type, the substrate having a substrate surface;

(b) a buried layer selectively formed in the substrate surface and diffused with a second material to give the buried layer the opposite conductivity type as the substrate;

(c) an epitaxial layer formed on the substrate surface and on the buried layer, the epitaxial layer having the opposite conductivity type as the substrate, the epitaxial layer having an epitaxial surface distal from the substrate surface;

(d) a first diffused region selectively formed on the epitaxial surface, the first diffused region having the same conductivity type as the epitaxial layer, the first diffused region having a first surface distal from the substrate surface;

(e) a second diffused region selectively formed on the first surface, the second diffused region having the opposite conductivity type as the first diffused region, the first diffused region and the second diffused region combine to form a first semiconductor junction; and

(f) a third diffused region selectively formed on the epitaxial surface remote from the first diffused region, the third diffused region having the opposite conductivity type as the epitaxial layer, the epitaxial layer and the third diffused region combine to form a second semiconductor junction.

12. The flip chip of claim 11, in which the first semiconductor junction operates in a reverse avalanche mode while the second semiconductor junction operates in a forward conducting mode during a transient over-voltage event.

13. The flip chip of claim 12, in which the epitaxial layer has a higher resistivity than the resistivity of the buried layer and in which a transient current is shunted through the buried layer during the transient over-voltage event.

14. The flip chip of claim 13, in which the second diffused region has a second surface distal from the substrate surface and in which the third diffused region has a third surface distal from the substrate surface, and in which the second surface and the third surface provide first and second external electrical contacts for the transient voltage suppression device.

15. The flip chip of claim 14, including a first aluminum region disposed on the second surface and a second aluminum region disposed on the third surface, and including two solder bump pads at the first aluminum region and two solder bump pads at the second aluminum region, and in which the two of the solder bump pads at the first aluminum region are electrically coupled to the second diffused region and the two of the solder bump pads at the second aluminum region are electrically coupled to the third diffused region.